IN THE CLAIMS:

1. (currently amended) A method for improving the performance of an a multi-stage RF power amplifier circuit having at least an input stage and an output stage, comprising:

sensing a collector current in an input stage transistor of said input stage;

feeding a current equal or proportional to said input stage transistor collector current to an output stage bias circuit to boost the bias of ~~an~~ said output stage;

wherein the input stage transistor is operated in a class AB mode, and said output stage is fed through a matching network.

2. (previously amended) The method of claim 1, wherein the input stage transistor collector current is sensed and fed to the output stage bias circuit via a current mirror.

3. (previously amended) The method of claim 2, wherein one transistor comprising said current mirror is connected in series with a transistor that itself forms a second current mirror with the input stage transistor.

4. (previously amended) The method of claim 3, wherein the amplifier circuit comprises plural bipolar junction transistors (BJTs).

5. (previously amended) The method of claim 3, wherein the amplifier circuit comprises plural field effect transistors (FETs).

6. (previously amended) The method of claim 3, wherein the amplifier circuit comprises a combination of BJTs and FETs.

7. (currently amended) A multi-stage power amplifier ~~transistor~~ circuit, comprising:

an input stage;

an output stage with a biasing circuit; and

a current mirror, which senses an input signal current in said input stage

and

feeds a current proportional to said input signal current to ~~an~~ said output stage biasing circuit.

8. (previously amended) The circuit of claim 7, wherein said current mirror includes at least one BJT.

9. (previously amended) The circuit of claim 7, wherein said current mirror includes at least one FET.

10. (previously amended) The circuit of claim 7, wherein transistors comprised within said circuit include both BJTs and FETs.

11. (currently amended) A method of adaptively boosting ~~the~~ an output stage bias of ~~an~~ a multi-stage power amplifier circuit, said multi-stage power amplifier comprising at least an input stage and an output stage having an output stage bias circuit for providing said output stage bias, said method comprising:

sensing an input signal in said input stage; and

boosting ~~an~~ said output stage bias with a current equal or proportional to the input signal sensed in said input stage.

12. (currently amended) The method of claim 11, wherein the input signal is an FR signal.

13. (previously amended) The method of claim 12, where the input signal is sensed by a current mirror.

14. (previously amended) The method of claim 13, where a collector current of an input stage BJT is mirrored by the current mirror and fed into an output stage biasing circuit.

15. (previously amended) The method of claim 13, where a drain current of an input stage FET is mirrored by the current mirror and fed into an output stage biasing circuit.

16. (previously amended) The method of claim 15, where the current mirror comprises BJTs.

17. (previously amended) The method of claim 15, where the current mirror comprises FETs.

18. (currently amended) A subcircuit, to be used in ~~an~~ a multi-stage amplification circuit having at least an input stage and an output stage, comprising:

an input sensor, arranged to sense, in said input stage, an input signal to the amplification circuit; and

an output stage booster, arranged to boost a bias of ~~an~~ said output stage of the amplification circuit in proportion to said input signal sensed in said input stage.

19. (currently amended) The subcircuit of claim 18, wherein the input signal is an RF signal.

20. (previously amended) The subcircuit of claim 19, where the input sensor is a current mirror.

21. (previously added) A bias boosting subcircuit for a multi-stage power amplifier circuit, said multistage power amplifier comprising at least an input stage and an output stage, said subcircuit comprising:

two matched BJTs in a first current mirror,

wherein the first current mirror senses a collector current of an amplifying transistor in the input stage, and feeds an equal or proportional current to a bias circuit of the output stage.

22. (previously added) The subcircuit of claim 21, where one of the transistors of the first current mirror is connected in series with a third transistor, said third transistor itself forming a second current mirror with the input stage amplifying transistor.

23. (previously added) The subcircuit of claim 22, where the first current mirror comprises two matched PNP BJTs, and the second current mirror comprises two matched NPN BJTs.

24. (previously added) The subcircuit of claim 23, where one transistor of the first current mirror has its collector connected to a collector of said third transistor.

25. (previously added) The subcircuit of claim 24 comprising further transistors and wherein a collector of at least one of said further transistors is contained within said first current mirror and is connected to a collector of an NPN transistor in the output stage.

26. (previously added) The subcircuit of claim 25, where said output stage also comprises an NPN transistor that is itself part of a current mirror.